ARCAM

BLACK BOX 500
D/A CONVERTOR
SERVICE MANUAL

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Issue 1 (Paul Newton/Simon Blandford May'94)

Arcam Drawing No. HO4/0023

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TECHNICAL SPECIFICATION

Conversion system		BITSTREAM with ARCAM custom 1bit DAC
Sampling rates accepted		32kHz, 44.1kHz, 48kHz
Dynamic range		108dB
Signal to noise ratio (CCIR)		110dB
Harmonic distortion (0dB)		0.01%
Frequency response (+/- 0.2dB)		1Hz - 20kHz
Output level (0dB)	Low output	2.4V RMS
	High output	5.0V RMS
Output impedance		33ohms
Minimum recommended load		1Kohm
Mains input		230V ± 12%
Power consumption		40VA
Size W/D/H mm.		430 x 295 x 95

Unit Function

The BB500 is a digital audio pre-amplifier which can convert one of seven digital audio inputs into an analogue audio output suitable for connection to an analogue pre-amplifier or directly to a power amplifier (such as the Arcam D120.2 or D290P). The output level is variable in 100 1dB steps. An independent record output is available to enable a digital recorder (such as DAT) to make recordings from any of the seven inputs regardless of which one is being monitored.

The input signal may be SPDIF format or AES/EBU format into any of the seven inputs. The AES/EBU uses different status flags, the BB500 acts on any flags it can e.g. de-emphasis. A clock signal for synchronising all the subsequent stages up to the DAC is extracted from the input signal.

For the DAC to function optimally, this clock signal must be very pure in terms of phase noise and jitter. To achieve this, three crystal oscillators cover clock frequencies required for three standard audio data sampling rates of 32KHz, 44.1KHz and 48KHz. The crystal oscillators can lock-in to the recovered clock using a phase locked loop system to produce a super-pure clock for the DAC itself and for re-clocking the record output, if it the same as the source output. The crystals have a narrow range and can only lock into input signals which have sampling frequencies accurate to +/- 50ppm, outside this range the rough clock must be used.

An even more pure clock can be obtained by running the crystal oscillators independently of the incoming signal clock as a master clock and slaving the source device to this reference. This is the Synclock system used by Arcam transports where an optical interface sends a clock at 64 times the sampling rate to the transport.

When a new signal is selected, the 12.288MHz crystal is activated to provide a 6.144MHz reference for the input decoder chip, Z701. This enables the input chip to measure the incoming sampling rate to find out which crystal clock, if any, can possibly be used for Class 1 mode or Synclock mode.

Having found the sampling frequency of the signal, Synclock is attempted. The optical synclock outputs are enabled and the phase detector, Z405, compares the crystal clock phase with the recovered clock to see if the recovered clock is synchronized. If the phase slips before a time-in period of about a second, then Synclock is aborted, otherwise the phase of the Synclock output is adjusted to ensure that the latches don't latch on data transitions.

If Synclock didn't work, then an attempt is made to lock the crystal oscillators to the recovered clock using a phase locked loop system. If lock is achieved for more than about a second, then the unit switches to Class 1 mode, otherwise the phase locked loop is kept active until it can lock, but the crystal clock is not used by the DAC.

If Synclock or Class 1 modes are achieved, the data coming out of the digital filter and

pulse encoder, Z704 and Z708, is latched twice with the purified clock signal. This reduces the phase noise and jitter present on the edges of the digital signal and improves the performance of the overall DAC by lowering the noise floor by a few dBs, reducing low level distortion and improving the subjective sound quality.

Note: Audio signals can be extracted from this digital signal simply by passing it through a low pass filter, all the way from the output of Z704 to the output of Z501 & Z551. Hence what looks like a digital signal on an oscilloscope, looks like audio on an Audio Precision Analyzer, for example. Set the low pass filter to <100KHz.

The edge-purified pulses emerging from Z502 and Z552 are then shaped so that the high level and low level of the pulse is free from ringing or any other deformation normally present on digital signals. It is this signal which is finally filtered in the analogue domain via Z101, Z102, Z201 and Z202.

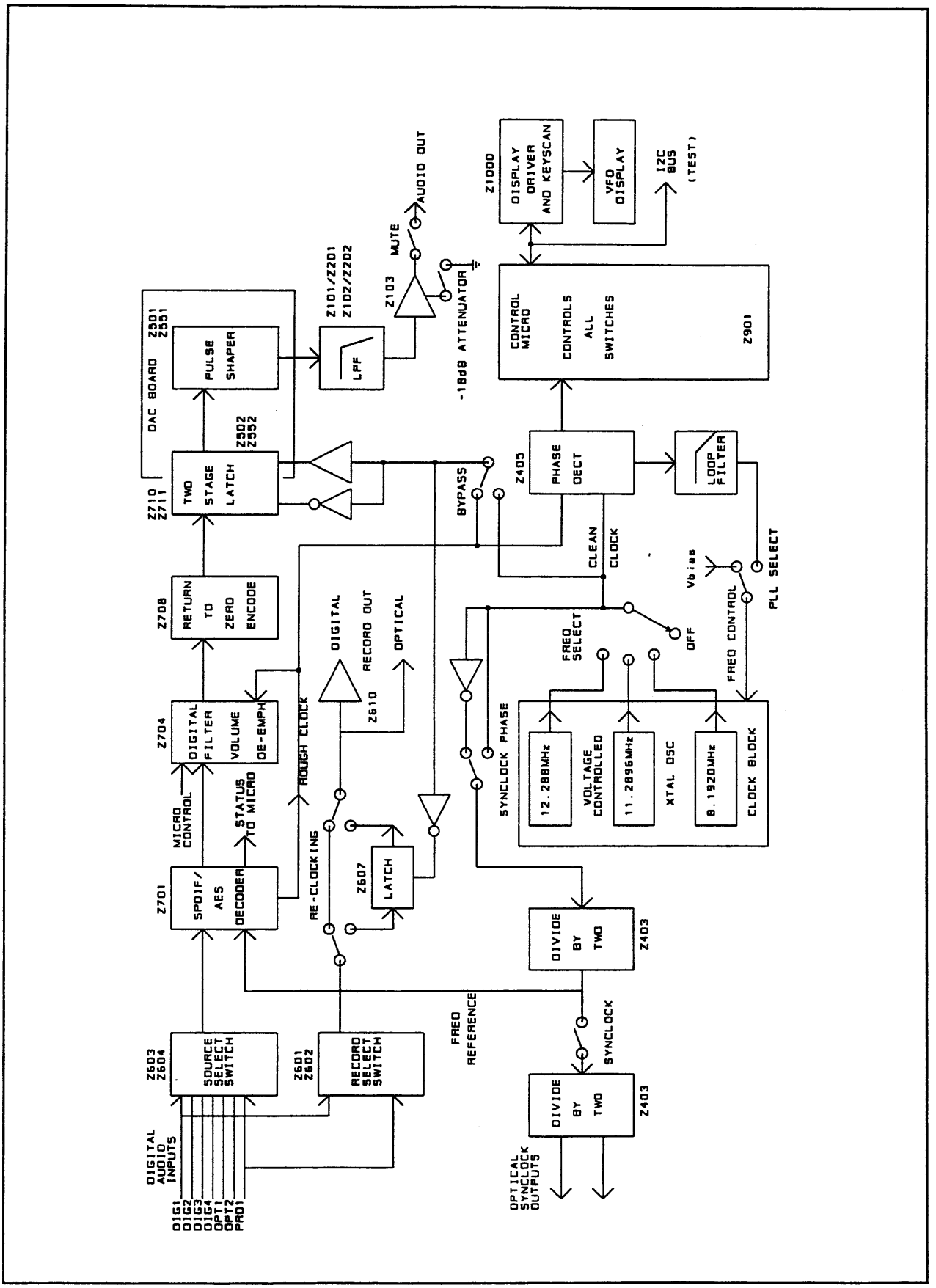


Figure 1 Block diagram of Black Box 500

Circuit Description

Input Switching (Circuit diagram sheet 4)

The coaxial inputs are loaded with 75R loads and de-coupled to the chassis. The signals from the optical inputs receivers are attenuated to match the levels from the coaxial inputs. The AES/EBU input is attenuated through a transformer and resistor network.

Both the live and neutral signals from the inputs are switched by CMOS analogue switches, Z601 and Z602 select the input for recording, Z603 and Z604 select the input for listening.

Z605 buffers the Record signal to standard CMOS levels. If the Record input is the same as the source input and the unit is in Class-1 mode, the Record signal is selected from Z607 by Z606-A, otherwise the Record signal is not re-clocked and is selected by Z606-B. If no record input is selected, Z606 A and B are de-selected. Z610 buffers the record signal to drive the coaxial output.

Digital Audio Decoding and Filter (Circuit diagram sheet 5)

Z701 receives the selected digital input signal and internally buffers it from SPDIF levels (pin 9 and 10). When a new signal is found, a 6.144MHz clock is applied to pin 13 (FREF). This is used to find the sampling rate of the signal. The error flags, frequency information and status bits are read by the micro.

Pin 28, VERF produces an output when the audio data is not valid and is used by the digital filter, Z704 to cover up unreliable data. This happens when a CD is being fast-forward, for example.

The rough clock is recovered by Z701.

Z606-C can break the audio data going into the digital filter. This happens as soon as a 'no signal' condition occurs to prevent any pops and clicks. Z709 can invert the data, but this is never ever done, and is effectively redundant.

The digital filter, Z704, converts the I^2S data from Z701 into the basic bitstream signal. It also does the digital de-emphasis and volume control and is controlled using a three-wire bus from the micro.

Z708 chopped the bitstream data from Z704 so that any '1' pulses are cut to half length i.e. they always return to zero. '0' pulses are unaffected. The chopped bitstream data is latched through Z710 and Z711, to the purified clock signal, if in Class-1 or Synclock mode, or to the rough clock otherwise.

Bitstream pulse purifier (Circuit diagram sheet 8)

The chopped and latched bitstream data from Z710 and Z711 is latched again by Z502 and Z552 to further reduce jitter on the data edges. Having eliminated the jitter from the edges of the data, the rise and fall time of the pulses are slowed and the high and low states are supplied from a clean source free from ringing and interference. This is achieved by using analogue switches Z502 and Z551 to switch the appropriate '0' or '1' level as required.

Clock block (Circuit diagram sheet 9)

The clock block contains three XTAL oscillators, none or one of which is selected at a time.To select one of the three XTAL circuits, a bias voltage is applied to the base of the appropriate transistor Q301, Q302 or Q303. This causes the transistor to start conducting through D301, D302 or D303 into R316. The other two diodes are left reversed biased so that the other two XTAL circuits remain isolated. The conducting transistor now acts as the active component in a Colpitts oscillator circuit. Two varicap diodes DV301 and DV302, for example, allow the frequency of the oscillator to be varied over a range of +/-100ppm by a control voltage, FCTRL.

Q304 buffers the clock signal followed by Z302-A and Z302-B.

The clock signal used to re-latch the bitstream data is selected by Z305. If Class 1 or Synclock mode is not established, then Z305-C and Z305-D selects the rough clock,

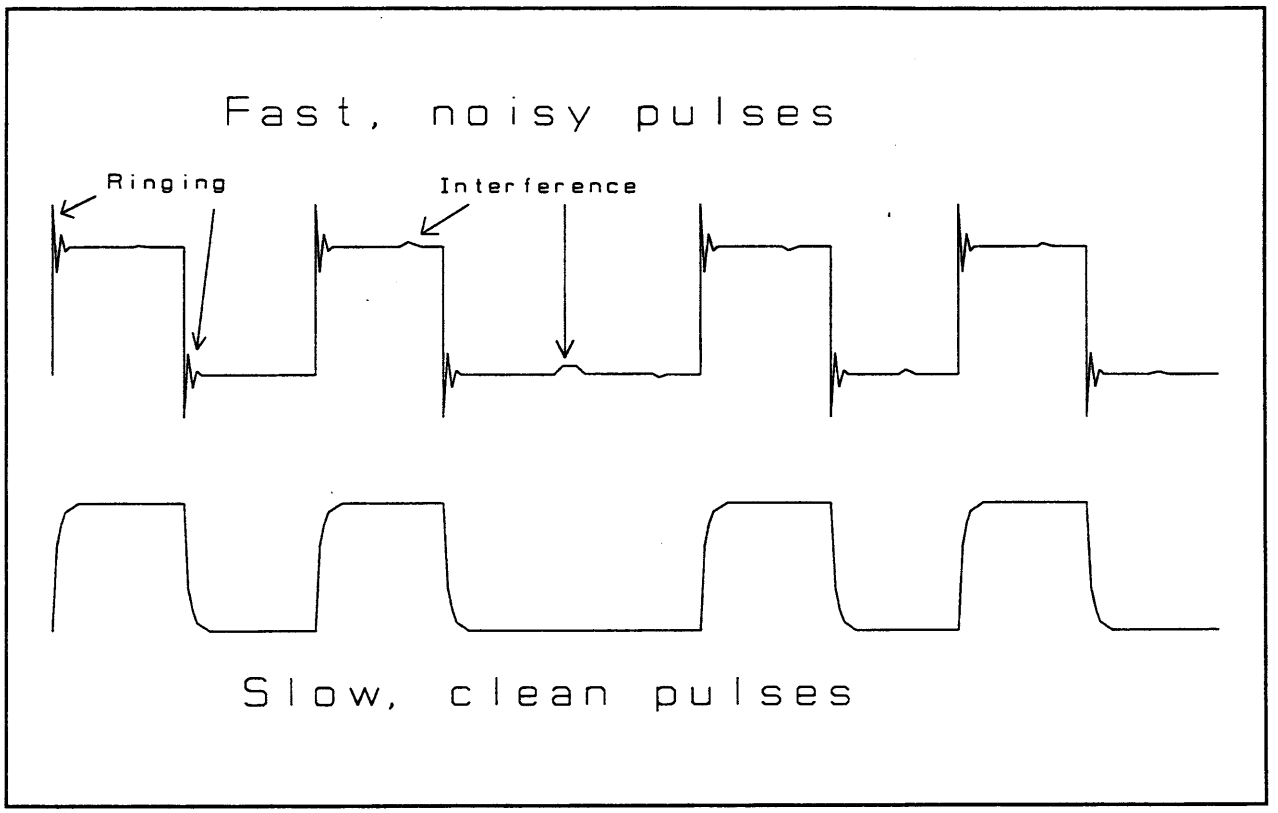


Figure 2 Pulse purifier effect

otherwise, Z305-A and Z305-B select an XTAL clock for re-latching.

Clock control unit (Circuit diagram sheet 3)

The XTAL clock is synchronised to the rough clock in one of two ways. In Synclock mode, the XTAL clock is divided by four by Z403 and sent to the digital transport via Z401 or Z404 optical transmitters. In this mode, Z405-B compares the phase of the XTAL clock with the rough clock and the DELTAF signal is used to determine the phase difference. If the transport is locked, this will be a d.c. value between 0 and 5V. The micro may invert the

phase of the clock being sent to the transport through Z709-B if the phase of the rough clock is such that the edges of the bitstream data from Z708 are too close to the clock low-to-high edges going to Z710 and Z711. If the transport is not locked, a triangle wave will be present at DELTAF at a frequency equal to the difference between the BB500 XTAL and the rough clock.

In Class-1 mode, Z405 phase/frequency output is filtered and drives a loop filter and transistor op-amp integrator, Q405, Q406, and Q404. The output from this filter is used to lock the phase and frequency of the XTAL clock to the rough clock. The FIXF signal disables the op-amp, when in Synclock mode, and fixes the XTAL frequency control voltage so that the centre frequency is selected. When the XTAL clock and rough clock are locked in phase, the LOCK signal is high to inform the micro all is well.

When the XTAL clock is selected, the BYPASS signal to Z407-B is low, this is the same signal used by Z305 in the clock block. This prevents the rough clock from being sent to the clock block when not required to prevent jitter being induced in the XTAL oscillator circuits.

Watch dog timer (Circuit diagram sheet 6)

In the event of the micro crashing, a watchdog timer, Q901 and Q902 will reset the micro. When the micro is running normally, pulses will be sent from pin 45 of the micro, Z901, to keep the watch dog quiet. A fault occurs if these pulses stop for more than about three seconds. After such time, Q901 and Q902 revert to being an astable multi-vibrator circuit and will send repeating reset pulses to pin 8 of the micro.

Audio Filter (Circuit diagram sheet 2)

The purified bitstream signal is filtered by a differential input four-pole low-pass filter Z102, Z101, Z202 and Z201. If a 0dB sine wave is being filtered, a corresponding signal should be visible pins 1 and 7 of Z102 and Z202 and pin 1 of Z101 and Z201. The d.c. servo voltage is available on pin 7 of Z101 and Z201 and is normally between 2 and 6 Vdc.

RL102 switches in a -18dB attenuator for low volume settings. This is then buffered by Z103 to drive the audio outputs.

Power Supplies (Circuit diagram sheet 1)

The BB500 has two power transformers - TX1 for the digital stage power supplies and TX2 for the analogue stage power supply.

The analogue supply provides +/- 15V regulated by Z1 and Z2 and their respective circuitry.

The digital supply provides +8V regulated, +27V regulated for the display driver and display and +4.7V regulated for the display filament heater d.c. bias. A separate tapping on the digital supply transformer is used to provide the filament heater a.c supplies.

The +8V rail is further regulated by additional +5V regulators at various points on the circuit to power the actual digital circuits (see individual circuits for more information).

Change of Mains Voltage

WARNING - the unit **must** be unplugged from the mains when replacing the fuse as the mains inlet and fuse are at mains potential even with the unit switched off.

The Black Box 500 can be set for use on 230v or 115v mains supplies.

There are 2 mains fuseholders in the unit - one marked 230v (F1) & the other 115v (F2) and the fuseholder with the fuse fitted to it determines the working voltage.

To change voltage remove the fitted fuse and fit the correct fuse to the other fuseholder.

The correct fuses are: 250 mA antisurge for 230v
500 mA antisurge for 115v

NOTE: ONLY FIT ONE FUSE AT A TIME!!

Test Points (marked on circuit diagrams)

Measurements made at 230V mains supply.

AGRND	Analogue ground	0	Vdc
ANAN16	Analogue regulated -ve supply	-15.3 +/- 0.5	Vdc
ANANPR	Analogue pre-regulated -ve supply (audio muted)	-22.0 +/- 1.0	Vdc
ANANUN	Analogue unregulated supply (audio muted)	-24.4 +/- 1.0	Vdc
ANAP16	Analogue regulated +ve supply	15.3 +/- 0.5	Vdc
ANAPPR	Analogue pre-regulated +ve supply (audio muted)	22.0 +/- 1.0	Vdc
ANAPUN	Analogue unregulated +ve supply	24.0 +/- 1.0	Vdc
BIT5V	Z710, Z711 5V supply	5.0 +/- 0.2	Vdc
BPASSN	Not bypass signal, high when Class 1 or Synclock active	0 = off, 5 = active	Vdc
BPASSP	Bypass signal, as above but inverted	"	"
DFCLK	Clock for Z711. Sampling rate times 256, square wave	5.0 +/- 0.5	Vpk
DIG1L	Coaxial SPDIF input, Dig 1, live	1.0 +/-0.2	Vpkpk
DIG1N	Neutral for above	0 relative to above	Vdc
DIG2L	Dig 2, live	"	"
DIG2N	Dig 2, neutral	"	"
DIG3L	Dig 3, live	"	"
DIG3N	Dig 2, neutral	"	"
DIG4L	Dig 4, live	"	"
DIG4N	Dig 4, neutral	"	"
DIGF5V	Digital filter, Z704 supply	5 +/- 0.2	Vdc
DIGGND	Digital section ground connection	0	Vdc
DIGNUN	Unregulated -ve digital supply	-14.8 +/-1.0	Vdc
DIGP8V	Pre-regulated +ve digital supply	8.2 +/- 0.5	Vdc
DIGPUN	Unregulated +ve digital supply	12.0 +/- 1.0	Vdc

DRPOUT	Mains OK detect, goes low as soon as mains is disconnected. Must be low before DIGP8V is less than 5V after mains is removed.	0 = mains interrupt, 4.7 = mains OK.	Vdc
DSILN	Bitstream input to DAC PCB, Left cold	0 & 5 +/- 0.2	Vpk
DSILP	Bitstream input to DAC PCB, left hot	"	"
DSIRN	As above, right cold	"	"
DSIRP	As above, right hot	"	"
DSMLN	Bitstream output from DAC PCB, left cold	0 & 4 +/-0.3	Vpk
DSMLP	As above, left hot	"	"
DSMRN	As above, right cold	"	"
DSMRP	As above, right hot	"	"
FCTRL	Voltage control of XTAL frequencies on DAC PCB. Centre frequency @8.5Vdc should be accurate to <40ppm. Range from 0.8 to 17.1Vdc should be >200ppm.	0.8 to 17.1 Signal & Class 1, 8.5 +/- 0.2 Synclock	Vdc
FSENSE	XTAL oscillator monitor output from one of three XTALs on DAC PCB if selected. Square wave, at one of three frequencies.	5 +/- 0.5	Vpk
I^2CCLK	I^2C Clock line. This is pulled high with a pull-up inside the micro. When clock pulses are sent this line is pulsed low.	5 +/- 0.5 (static)	Vdc
I^2CDAT	I^2C Data line. Same conditions as above.	5 +/- 0.5 (static)	Vdc
KEYINT	Key pressed interrupt. Low = keypress waiting for micro.	0=key, 5=No key	Vdc
LAUDHI	Left audio output	0dB = 2.3 +/- 0.1	Vrms
LAUDLO	Left audio output	0dB = 2.3 +/- 0.1	Vrms
LED32K	32K LED drive	0 & 2(on) +/- 0.5	Vdc
LED44K	44.1K LED drive	"	"
LED48K	48K LED drive	"	"
LEDPWR	Power LED drive	"	"
LEDSIG	Signal LED drive	"	"
LEDSYN	Synclock LED drive	"	"
LEDVCO	Class 1 LED drive	"	"

MPU5V	Micro, Z901, supply. Should remain present for several days after unit is switched off. (measure with high impedance meter! e.g. Fluke)	5 +/- 0.5 (on), >3 after mains off for 24 hours	Vdc
MPURST	Micro reset signal. Low = reset.	0 & 5 +/- 0.5	Vdc
OPT5V	Optical inputs, Z613 & Z614 supply	5 +/- 0.2	Vdc
OSC32N	DAC PCB 8.1920MHz XTAL oscillator select	0 = on, 5 = off	Vdc
OSC44N	As above, for 11.2896MHz	"	"
OSC48N	As above for 12.2880Mhz	"	"
PHSP5V	Phase detector, Z405 supply	5 +/- 0.2	Vdc
PROIL	AES/EBU input live	3 to 10	Vpkpk
PROIN	AES/EBU input neutral	0 relative to above	Vdc
RAUDHI	Right audio output	0dB = 2.3 +/- 0.1	Vrms
RAUDLO	Right audio output	0dB = 2.3 +/- 0.1	Vrms
RCOSC	Rough clock input to DAC PCB, square wave @ 256 sampling rate. Active when BPASSP = high.	5 +/- 0.3	Vpk
RECLK	Clock for record output, Z607. Square wave at 256 times sampling rate.	5 +/- 0.3	Vpk
RECN5V	Record output buffer, Z610, -ve supply	-5 +/- 0.2	Vdc
RECOL	Coaxial SPDIF record output, live. Active when record select is monitoring a valid digital audio input.	700 +/- 50, 75R load	mV pkpk
RECON	Neutral for above	0	Vdc
RECP5V	Record output buffer, Z610, +ve supply	5 +/- 0.3	Vdc
RMODE	Remote control mode switch, Low = in, high = out	0 & 5 +/- 0.2	Vdc
SCLOCK	Clock for Synclock and sampling rate measurement. Square wave at 256 times sampling rate.	5 +/- 0.3	Vpk
SPDIF5V	Input decoder supply, Z701	5 +/- 0.2	Vdc
SW5V	Input switching supply Z601 to Z605	5 +/- 0.2	Vdc
SYNP5V	Synclock system supply	5 +/- 0.2	Vdc
NTEST	MIcro self test. Stays low if test fails, high when test passes. Valid >3 seconds after mains switched on.	0 = fail, 5 = pass +/- 0.3	Vdc
VCO5V	Supply for VCO on Z701	5 +/- 0.2	Vdc
VCP17V	Supply for VCXO loop filter	16.7 +/- 0.5	Vdc

VCXPPR	Pre-regulated supply for VCXO loop filter	32.0 +/- 2	Vdc
VFD4V7	VFD 4.7v bias for heater supply	4.7 +/- 0.5	Vdc
VFD27V	Supply for VFD driver and display	28.2 +/- 1	Vdc
VFDAC1	VFD AC heater supply #1	6.5 +/- 1 bias 1.8 +/- 0.4 supply	Vdc Vrms
VFDAC2	VFD AC heater supply #2	6.5 +/- 1 bias 1.8 +/- 0.4 supply	Vdc Vrms
VFDUN	VFD and VCXO loop filter supply, unregulated	32.5 +/- 2	Vdc

Board Connections

SK101 Phono digital audio coaxial input,4x audio 0dB = 2.3Vrms,

Z401 Optical Synclock output #1, RCZ-6901 standard connector.

Z402 Optical Synclock output #2, RCZ-6901 standard connector.

SK601 BNC 75R coaxial digital audio record output, SPDIF standard.

Z608 Optical digital audio output, RCZ-6901 connector.

SK602 Digital audio input #1, BNC 75R, SPDIF standard.

SK603 Digital audio input #2, BNC 75R, SPDIF standard.

SK604 Digital audio inputs #3 & #4, Phono 75R, SPDIF standard.

Z613 Optical digital audio input, RCZ-6901 connector.

Z614 Optical digital audio input, RCZ-6901 connector.

PL601 Digital audio input, XLR socket, AES/EBU standard.

PL1 115 or 230V +/-12%, 55-65Hz power inlet, IEC socket.

PL901		Connection to display PCB, 16 pin DIL IDC locking male header
Pin	**Type**	**Function**
1	Pwr O	0v Connection
2	Pwr O	VFD AC supply #1, 6.5V +/- 1V d.c. + 1.8V +/- 0.4V rms
3	Pwr O	VFD AC supply #2, 6.5V +/- 1V d.c. + 1.8V +/- 0.4V rms
4	Pwr O	+27V DC supply for VFD display driver and display
5	I/O	I^2C bus data line to display and keyscan driver
6	I/O	I^2C bus clock line to display and keyscan driver
7	I	'Key-pressed' interrupt line
8	O	'Power' LED drive
9	O	'48K' LED drive
10	O	'44.1K' LED drive
11	O	'32K' LED drive
12	O	'CLASS 1' LED drive
13	O	'SIGNAL' LED drive
14	O	'SYNCLOCK' LED drive
15	I	RC5 remote control codes
16	Pwr O	+8V supply for remote RX IC

PL903		Test socket for OSD diagnostics, JST 4way
Pin	**Type**	**Function**
1	I/O	I^2C clock line to OSD test unit, 5V static, 0V pulses active
2	I/O	I^2C data line to OSD test unit, 5V static, 0V pulses active
3	Pwr O	0V connection for OSD test unit
4	Pwr O	+8V supply for OSD test unit

PL701		DAC/Clock PCB digital return to zero bitstream code send
Pin	**Type**	**Function**
1	O	Pulse stream, DSILN, left, -ve, 5V pulses, 75 to 120μs
2	O	Pulse stream, DSILP, left, +ve, 5V pulses, 75 to 120μs
3	Pwr O	+15V supply to DAC PCB
4	Pwr O	+8V supply to DAC PCB
5	O	Pulse stream, DSIRN, right, -ve, 5V pulses, 75 to 120μs
6	O	Pulse stream, DSIRP, right +ve, 5V pulses, 75 to 120μs

PL101		DAC/Clock PCB return to zero bitstream code return
Pin	**Type**	**Function**
1	I	Pulse stream, DSMLN, left, -ve, 4V pulses, 75 to 120μs
2	I	Pulse stream, DSMLP, left, +ve, 4V pulses, 75 to 120μs
3	Pwr O	0v DAC and Clock PCB Reference
4	Pwr O	0V DAC and Clock PCB Reference
5	I	Pulse stream, DSMRN, right, -ve, 4V pulses, 75 to 120μs
6	I	Pulse stream, DSMRP, right +ve, 4V pulses, 75 to 120μs

PL402		DAC/Clock PCB Clock signal I/O
Pin	**Type**	**Function**
1	I	Record output clock, 7 to 13MHz square wave, 5V peak
2	I	Latch #1 clock, 7 to 13MHz, square wave, 5V peak
3	I	Synclock clock, 7 to 13MHz, square wave, 5V peak
4	I	Phase detect clock, 7 to 13MHz square wave, 5V peak
5	O	Rough clock, 7 to 13MHz square wave, 5V peak
6	Pwr O	+8V supply to Clock Block

PL902		DAC/Clock PCB Clock Control
Pin	**Type**	**Function**
1	O	Freq control voltage, 1 to 16Vdc Class 1 mode, 8.1 to 8.9Vdc Synclock mode
2	O	0V = select 12.2880Mhz osc., 5V = de-select
3	O	0V = select 11.2896MHz osc., 5V = de-select
4	O	0V = select 8.19200MHz osc., 5V = de-select
5	O	0V = select XTAL operation, 5V = bypass XTAL clock
6	O	0V = bypass XTAL clock, 5V = select XTAL operation

Service test mode

A manual test mode is provided to assist in service fault diagnosis. In this mode it is possible to force and hold a certain state, such as Synclock or Audio mute, without the micro responding to signal drop-outs and Synclock interruption as it would normally automatically do. It is also possible to measure the crystal frequencies at their centre frequencies and lowest and highest extremes.

To access this special mode, press **RECORD** then **DISPLAY**. The **PROGR** segment on the left of the VFD display lights up to indicate the first level of security has been reached. Two levels are needed to prevent accidental user access. Then press **RECORD** then **VOLUME DOWN**. The VFD display now changes completely, The new role of the display is shown in figure 2.

The digits show the value that the selected crystal frequency should be. If a frequency extreme is selected then the frequency display is modified to shows the +/- 100ppm value. These values are for a guide only - the actual frequency has to be measured with a high resolution frequency counter. The LEDs show which XTAL is selected for 32K, 44.1K or 48K. The Signal LED indicates that a valid signal is being received.
The front panel buttons now have different functions:

The Dig 1 - 3 buttons are the crystal frequency select.
Dig 4 is no crystal frequency.
Pro 1 is the DIRECT switch which switches on the rough clock. If DIRECT is not lit on the display the selected crystal will try to latch onto the audio data.
The display button is PLAY and activates the output relays. A flashing PLAY on the display indicates the -18 dB mute is on.
OPT 1 is the VCO TRACK on and using this the vco will try to lock to the incoming signal.
OPT 2 is the Synclock DIGOUT ON and forces the Synclock output on when the DIGOUT ON is lit on the display.
The volume buttons give a guide to the upper and lower extremes that the selected crystal frequency should be within. Volume up is the highest extreme and volume down the lowest

extreme.

Here is how to force various modes of operation, ensure that only the segments indicated below are illuminated and all others are cancelled.

Before entering service mode you must select the input you wish to check because it cannot be selected in service mode.

Signal mode

Select no XTAL 0 (Dig 4), DIRECT (Pro 1) and Audio PLAY (Display).

Class-1 mode

Select appropriate XTAL (Dig 1 to Dig 3), VCO TRACK (Opt 1), and Audio PLAY (Display). To simulate a Class-1 'out of lock' condition, select an XTAL other than the appropriate one for the current signal sampling rate. The FCTRL signal should swing to an extreme value (0.5 or 17.0V) and the LOCK signal should be 0V.

Synclock mode

Select appropriate XTAL (Dig 1 to Dig 3), Synclock DIGOUT ON (Opt 2), and Audio PLAY (Display). It is sometimes useful to force a Synclock 'fail' situation by de-selecting the Synclock output so that DIGOUT ON is not lit. In this mode there should be pulses on the

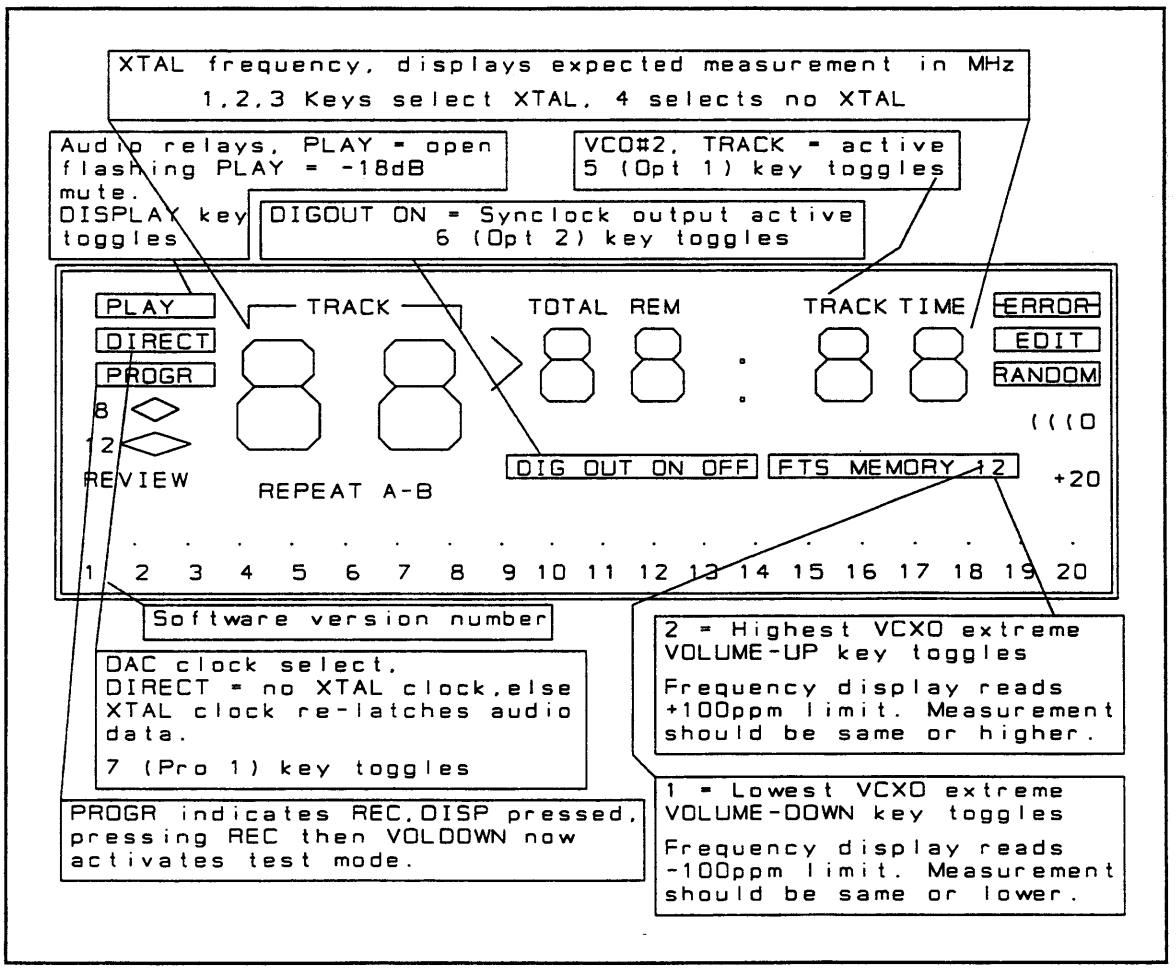


Figure 3 VFD display when in Special test mode

DELTAF line, Z901, pin 6. These pulses are normally used by the micro to deduce that Synclock is not working.

Microprocessor pin by pin description

Since the micro is connected to most important areas of the unit, a lot of diagnostic information can be deduced from its pins with an oscilloscope. The table is shown below lists all the pins and describes the activity on them.

1	**DATFILT**	I/O	The data line of a three-wire serial interface to the Digital Filter chip. Information is sent to control the filter mode and volume. This line should be active when a new signal is found or the volume control is adjusted. Static high, pulses low and high when data is sent.
2	**CLKFILT**	O	The clock signal for the above data. Static low, pulses high to clock data.
3	**RABFILT**	O	The latch-in signal for the above data. Static high, low when data is being sent.
4	**LOCK**	I	Indicates if the XTAL PLL is locking properly. High when locked or low with no signal, sawtooth waveform when only in Signal mode.
5	**REMOTE**	I	RC5 codes received from display board.
6	**DELTAF**	I	Output from phase detector. Indicates phase of XTAL relative to incoming clock as a dc signal The closer the phase the lower the voltage (In service mode only a triangular waveform can be seen when not locked but close to the incoming clock.)
7	**ERF**	I	Data error flag from SPDIF decoder. Causes immediate mute and loss of signal status.
8	**NRES**	I	Resets micro when low
9	**XTAL**	O	Chip clock resonator pin
10	**EXTAL**	I	Chip clock resonator pin
11	**MODE 1**	I	Used to set micro mode to use internal RAM and ROM and make as many IO pins available as possible. Single chip mode. Held high.
12	**MODE 0**	I	Used in conjunction with above. Held high.
13	**NMNI**	I	Key-press interrupt pin. Low indicates a key has been pressed on the display board.
14	**VCC**	PWR	+5v power supply to micro. C908 stores power to supply the micro RAM when the BB500 is disconnected from mains.
15	**NSTBY**	I	Low sends micro to sleep. This happens as soon as mains power is interrupted so that the volume, source and record selections can be saved in micro RAM.

16	VSS	PWR	0v connection to micro
17	SRC0	O	Source selection bit 0 for Z603 and Z604
18	SRC1	O	Source selection bit 1
19	SRC2	O	Source selection bit 2
20	REC0	O	Record selection bit 0 for Z601 and Z602
21	REC1	O	Record selection bit 1
22	REC2	O	Record selection bit 2
23	n/c		
24	n/c		
25	CE/F2	I	Channel or frequency information from SPDIF decoder, Z701
26	CD/F1	I	"
27	CC/F0	I	"
28	CB/E2	I	Channel or error information from SPDIF decoder
29	CA/E1	I	"
30	NC0/E0	I	"
31	FLSEL	O	Selects whether channel or frequency and error information is output from Z701 in above signals
32	PHASE	O	Selects data phase. Not implemented in software.
33	DIGSEL	O	Selects digital audio input for digital filter
34	ADCSEL	O	Selects monitor source for digital filter
35	CLKSUB	O	Subcode clock for digital filter, not implemented in software
36	DATAO	O	Subcode data for digital filter, not implemented in software
37	I^2CDAT	I/O	Data line to and from VFD display/keyscan driver and OSD test jig
38	I^2CCLK	I/O	Clock line for above data
39	VCC	PWR	Another power supply pin
40	RETHRU	O	Selects record output bypassing latch, Z607
41	RELTCH	O	Selects record output through latch, Z607
42	FIXF	O	Sets Voltage controlling frequency for XTAL oscillators to centre position +/- 40 ppm

43	FPULL	O	+/- 100ppm frequency test. 0V : +100ppm, 5V : -100ppm, z : norm
44	N18dB	O	-18dB Audio output attenuator relay
45	WDOG	O	Watch dog timer pulses. No pulses cause time-out.
46	NTEST	O	Signals a micro self-test failure . Low = fail, high = pass.
47	AUDIO	O	Opens the output mute relays when high
48	VSS	PWR	Another supply pin
49	RMODE	I	Selects remote control mode from SW901
50	LEDSYN	O	Drive for SYNCLOCK LED
51	LEDSIG	O	Drive for SIGNAL LED
52	LEDVCO	O	Drive for CLASS 1 LED
53	LED32K	O	Drive for 32KHz sampling rate LED
54	LED44K	O	Drive for 44.1KHz sampling rate LED
55	LED48K	O	Drive for 48KHz sampling rate LED
56	LEDPWR	O	Drive for power LED
57	NOSC32	O	Selects 8.19200MHz XTAL when low
58	NOSC44	O	Selects 11.2896MHz XTAL when low
59	NOSC48	O	Selects 12.2880MHz XTAL when low
60	NBYPASS	O	XTAL clock bypassed for DAC when low, compliment of above
61	BYPASS	O	XTAL clock bypassed for DAC when high
62	SILENCE	I	Signal from digital filter, Z704, indicating digital silence. Causes reset of the digital filter's DC filter. See DCHLD flag on OSD screen.
63	SYN-CLOCK	O	Enables output from Z401 and Z404 of synclock clock signal
64	CLKPHS	O	Inverts phase of synclock clock output to ensure incoming data latches through Z711 and Z607 at correct data-to-clock phase

Disassembly for Service

CAUTION - ANTI STATIC PRECAUTIONS MUST BE OBSERVED

1. Remove the top cover by removing 2 side screws from each side and 4 rear panel screws (2 along the top edge and one at each end). Slide the cover backwards and up away from the unit.

Removal of Main Circuit Board

1. Remove 5 screws from the pcb (3 along the front edge, 1 near the mains inlet and 1 between the transformers).

2. Remove 2 screw from the bottom edge of the rear panel.

3. Disconnect the lead going to the display board .

The board should now be free of the chassis with the rear panel attached.

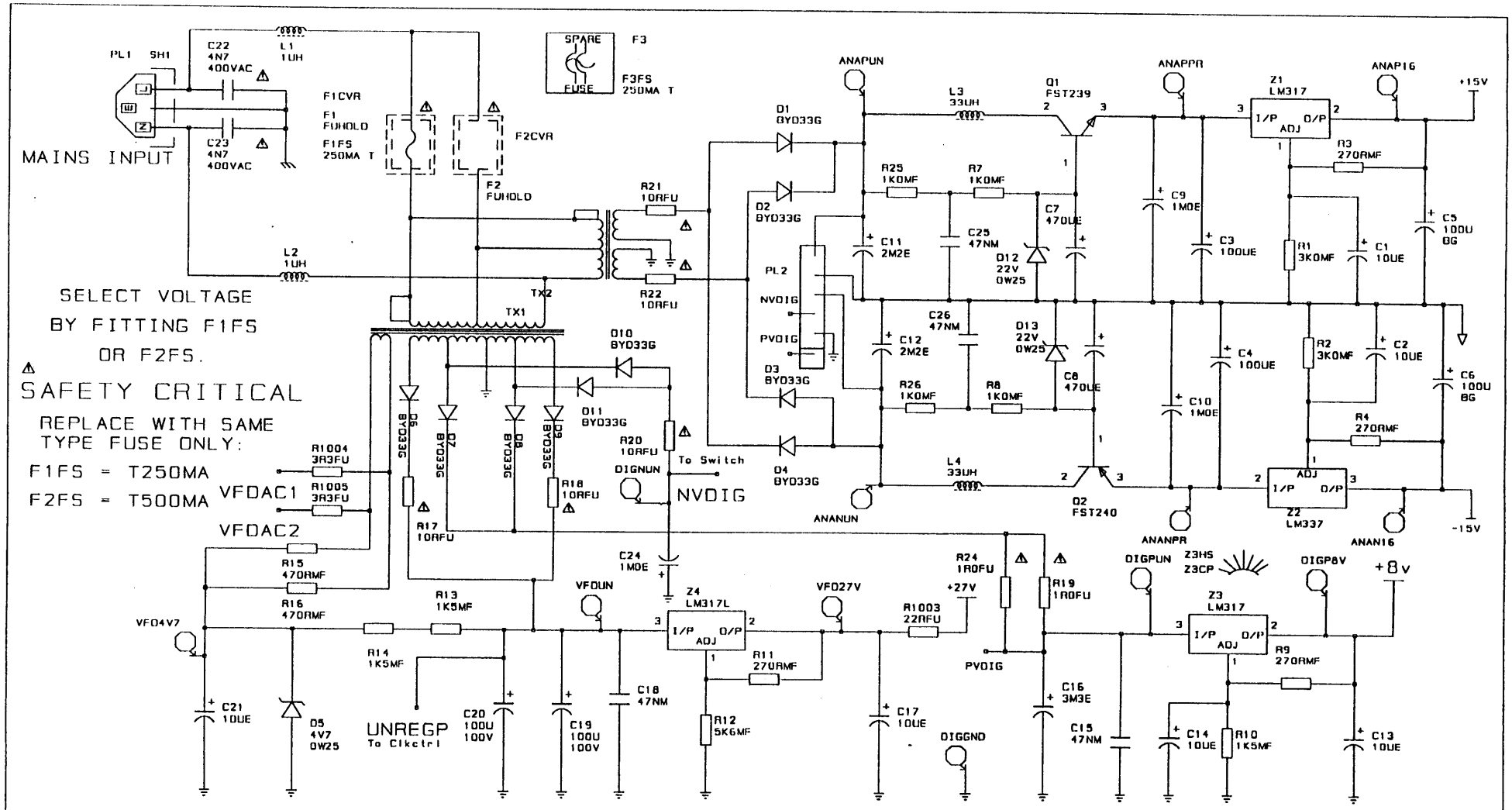
The clock/DAC board in the "tin can" can be removed if required by pulling upwards and pulling the board of its 4 six way connectors.

Removal of display PCB.

1. Remove the top cover.

2. Remove the front panel by undoing 4 screws (2 from each end) and pulling the front off taking care not to damage the control buttons or switches.

3. The display pcb can now be removed by undoing 7 screws from the front of the pcb and releasing the lead going to the main board.



ARCAM

A & R CAMBRIDGE LTD.
WATERBEACH
CAMBRIDGE
CB5 9PB

DRAWING TITLE

Black Box 500
Power Supply

701CT1.CSD

ISSUE	INITIALS	DATE	DESCRIPTION OF CHANGE	ECO No
1	SJB	21-6-94		

DRAWING TYPE Circuit Diagram

DRAWN WITH REFERENCE TO BS 308

ALL DIMENSIONS IN MILLIMETERS UNLESS OTHERWISE STATED

ORIGINAL SCALE A3

DRAWN BY SJB

DATE 12-11-93

CHECKED BY

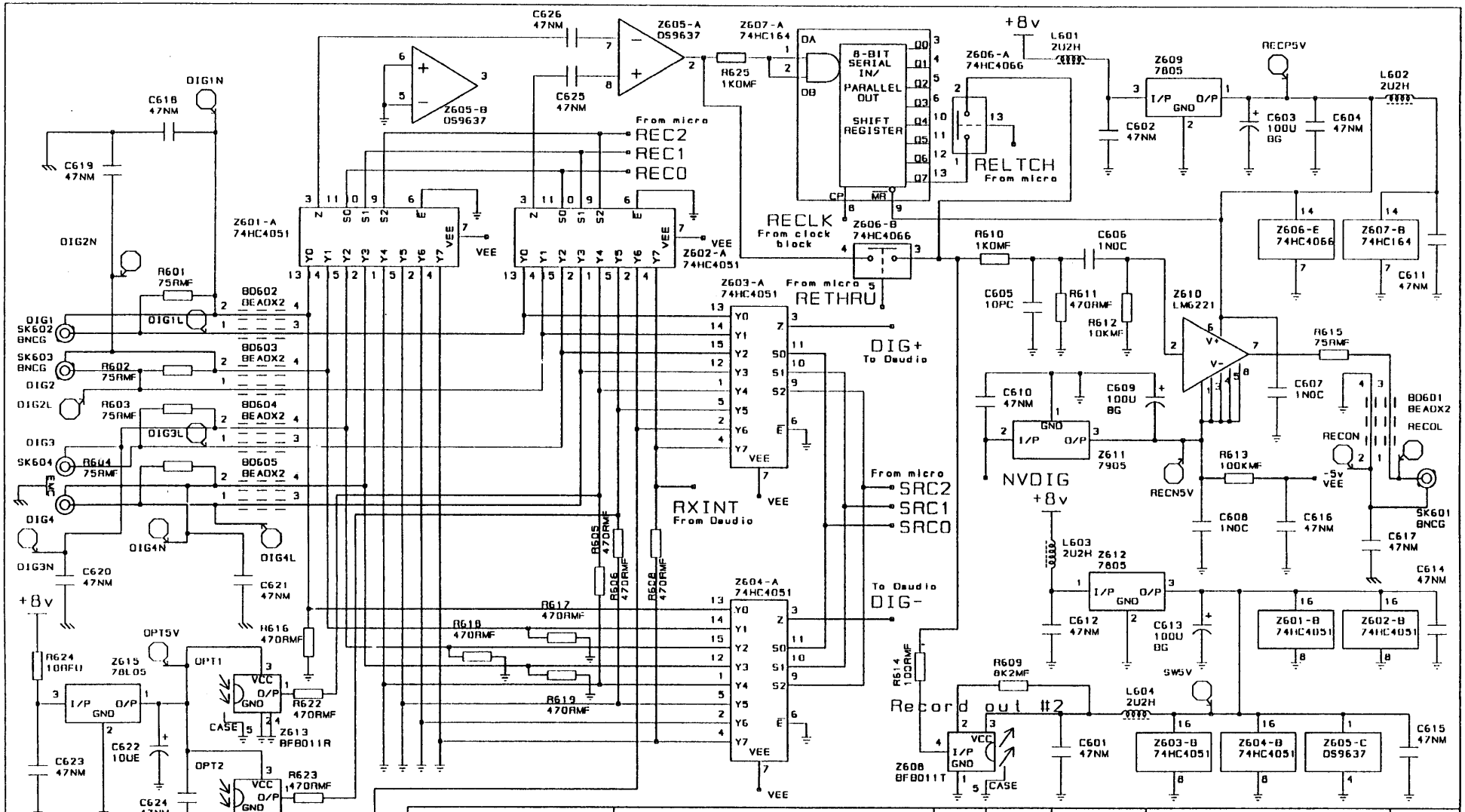
DATE

TOLERANCES

SHT 1 OF 7

PART/DRG No. L701CT1

List of Circuit Diagrams
Power Supplies
Analogue Filter
Clock Control Circuit & PLL 2
Input Switching
Digital Audio Decode/Encode & Filtering
Microcontroller
Keyboard & Display Board
Bitstream Pulse Purifier
Voltage Controlled Crystal Clock Block



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CB5 9PB

DRAWING TITLE

Input Switching

L701CT4.CSD

ISSUE	INITIALS	DATE	DESCRIPTION OF CHANGE	ECO No
1	SJB	13-5-94		

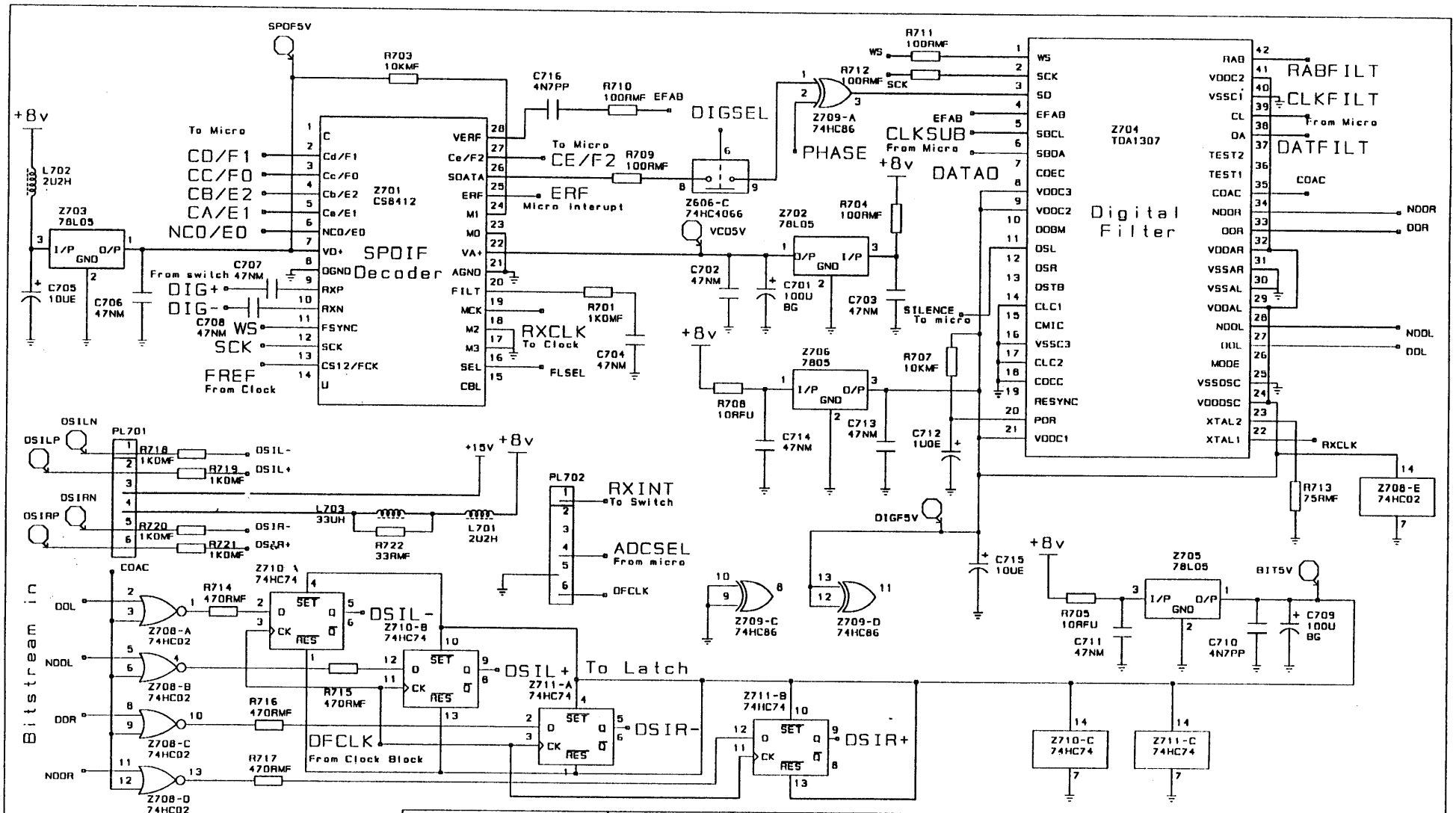
ALL DIMENSIONS IN MILLIMETERS UNLESS OTHERWISE STATED | ORIGINAL SCALE A3

TOLERANCES

DRAWING TYPE Circuit Diagram | DRAWN WITH REFERENCE TO BS 308

DRAWN BY SJB | DATE 23-9-93 | CHECKED BY | DATE

SHT 4 OF 7 | PART/DRG No. L701CT4



Return-to-zero chopper

For DAC/CLOCK PCB

SD701 16MM SPACER
SD702 16MM SPACER
SD703 16MM SPACER
SD704 16MM SPACER

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WATERBEACH
CAMBRIDGE
CB5 9PB

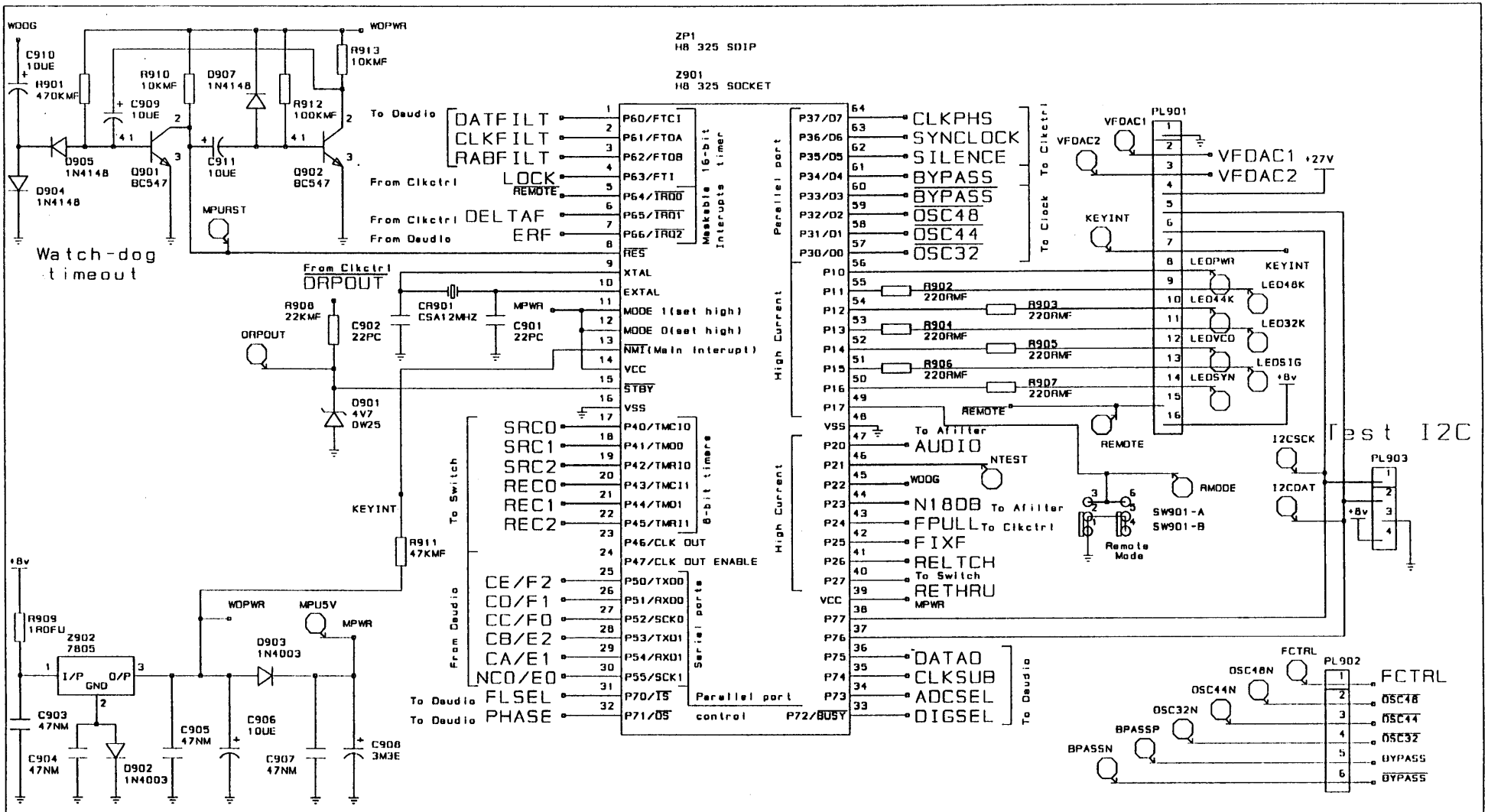
DRAWING TITLE
Digital Audio Decode/Encode And Filtering

L701CT5.CSD

ISSUE	INITIALS	DATE	DESCRIPTION OF CHANGE	ECO No
1	SJB	21-6-94		

ALL DIMENSIONS IN MILLIMETERS UNLESS OTHERWISE STATED
ORIGINAL SCALE A3
TOLERANCES

DRAWING TYPE Circuit Diagram
DRAWN WITH REFERENCE TO BS 308
DRAWN BY SJB
DATE 27-9-93
CHECKED BY
DATE
SHT 5 OF 7
PART/DRG No. L701CT5



1	SJB	13-5-94		
ISSUE	INITIALS	DATE	DESCRIPTION OF CHANGE	ECO No

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WATERBEACH
CAMBRIDGE
CB5 9PB

DRAWING TITLE: Microcontroller

L701CT6.CSO

DRAWING TYPE: Circuit Diagram

DRAWN WITH REFERENCE TO BS 308

ALL DIMENSIONS IN MILLIMETERS UNLESS OTHERWISE STATED | ORIGINAL SCALE A3

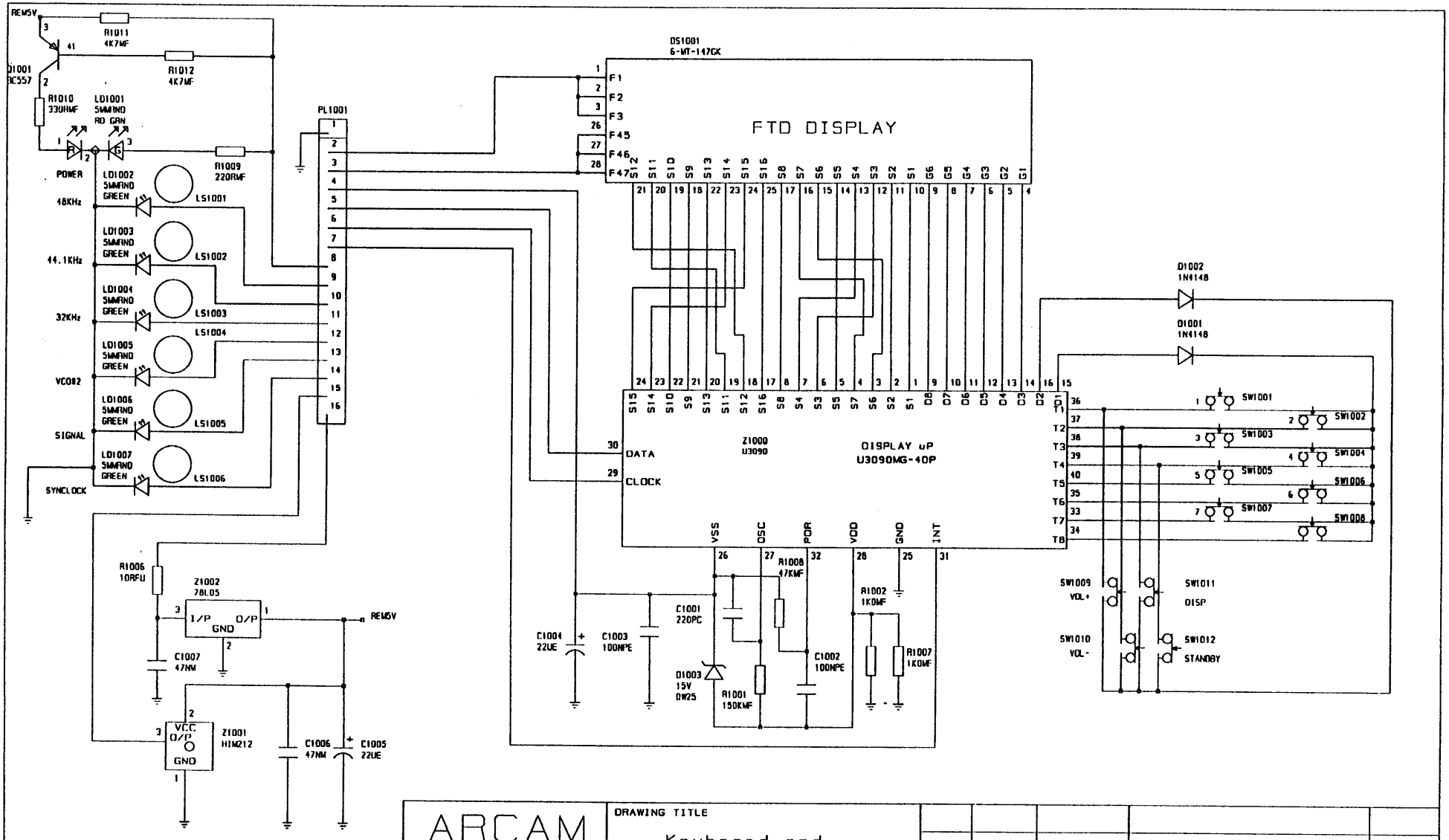
DRAWN BY SJB | DATE 2-12-93

CHECKED BY | DATE

TOLERANCES

SHT 6 OF 7

PART/DRG No. L701CT6



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CB5 9PB

DRAWING TITLE

Keyboard and Display PCB

L701CT7.CSD

ISSUE	INITIALS	DATE	DESCRIPTION OF CHANGE	ECO No
1	SJB	13-5-94		

DRAWING TYPE Circuit Diagram

DRAWN WITH REFERENCE TO 85 308

ALL DIMENSIONS IN MILLIMETERS UNLESS OTHERWISE STATED

ORIGINAL SCALE A3

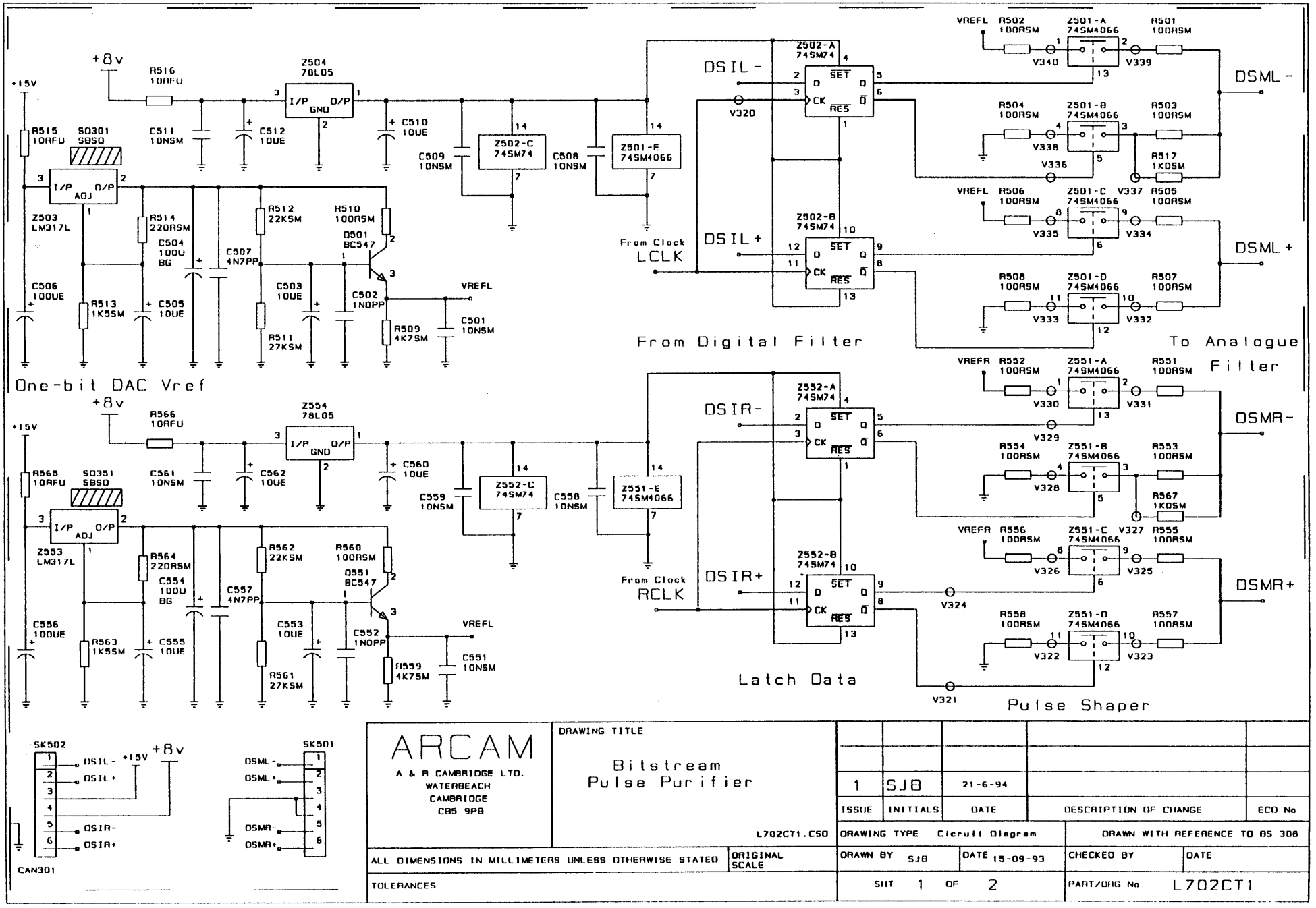
TOLERANCES

DRAWN BY SJB DATE 29-9-93

CHECKED BY DATE

SHT 7 OF 7

PART/ORG No. L701CT7



ARCAM

A & R CAMBRIDGE LTD.
WATERBEACH
CAMBRIDGE
CB5 9PB

DRAWING TITLE

Bitstream
Pulse Purifier

L702CT1.CSD

ISSUE	INITIALS	DATE	DESCRIPTION OF CHANGE	ECO No
1	SJB	21-6-94		

DRAWING TYPE Circuit Diagram

DRAWN WITH REFERENCE TO BS 308

ALL DIMENSIONS IN MILLIMETERS UNLESS OTHERWISE STATED

ORIGINAL SCALE

DRAWN BY SJB

DATE 15-09-93

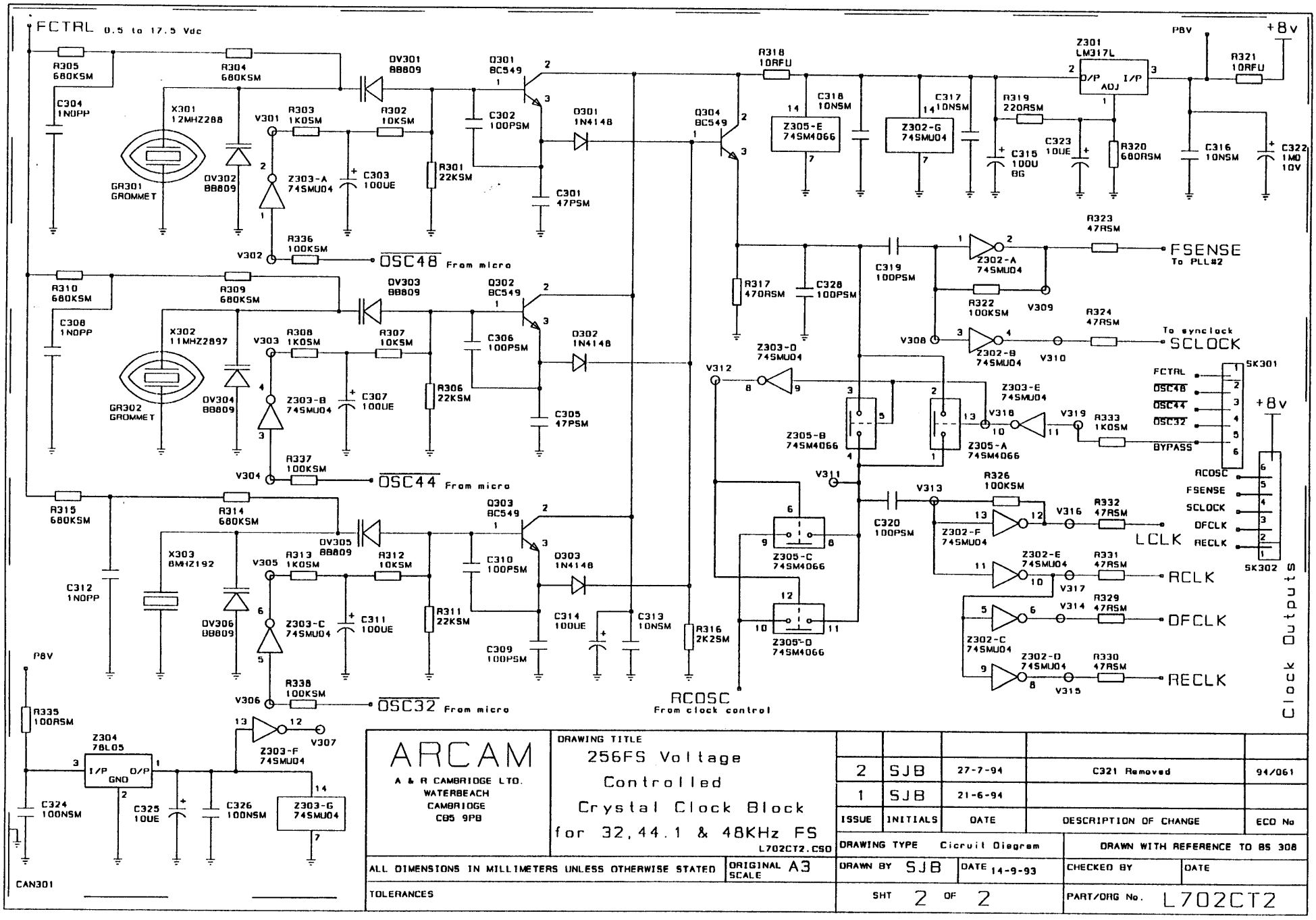
CHECKED BY

DATE

TOLERANCES

SHT 1 OF 2

PART/ORD No. L702CT1



ARCAM

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WATERBEACH
CAMBRIDGE
CB5 9PB

DRAWING TITLE

256FS Voltage Controlled Crystal Clock Block for 32, 44.1 & 48KHz FS

L702CT2.CSO

ISSUE	INITIALS	DATE	DESCRIPTION OF CHANGE	ECO No
2	SJB	27-7-94	C321 Removed	94/061
1	SJB	21-6-94		

ALL DIMENSIONS IN MILLIMETERS UNLESS OTHERWISE STATED

ORIGINAL SCALE A3

TOLERANCES

DRAWING TYPE Circuit Diagram

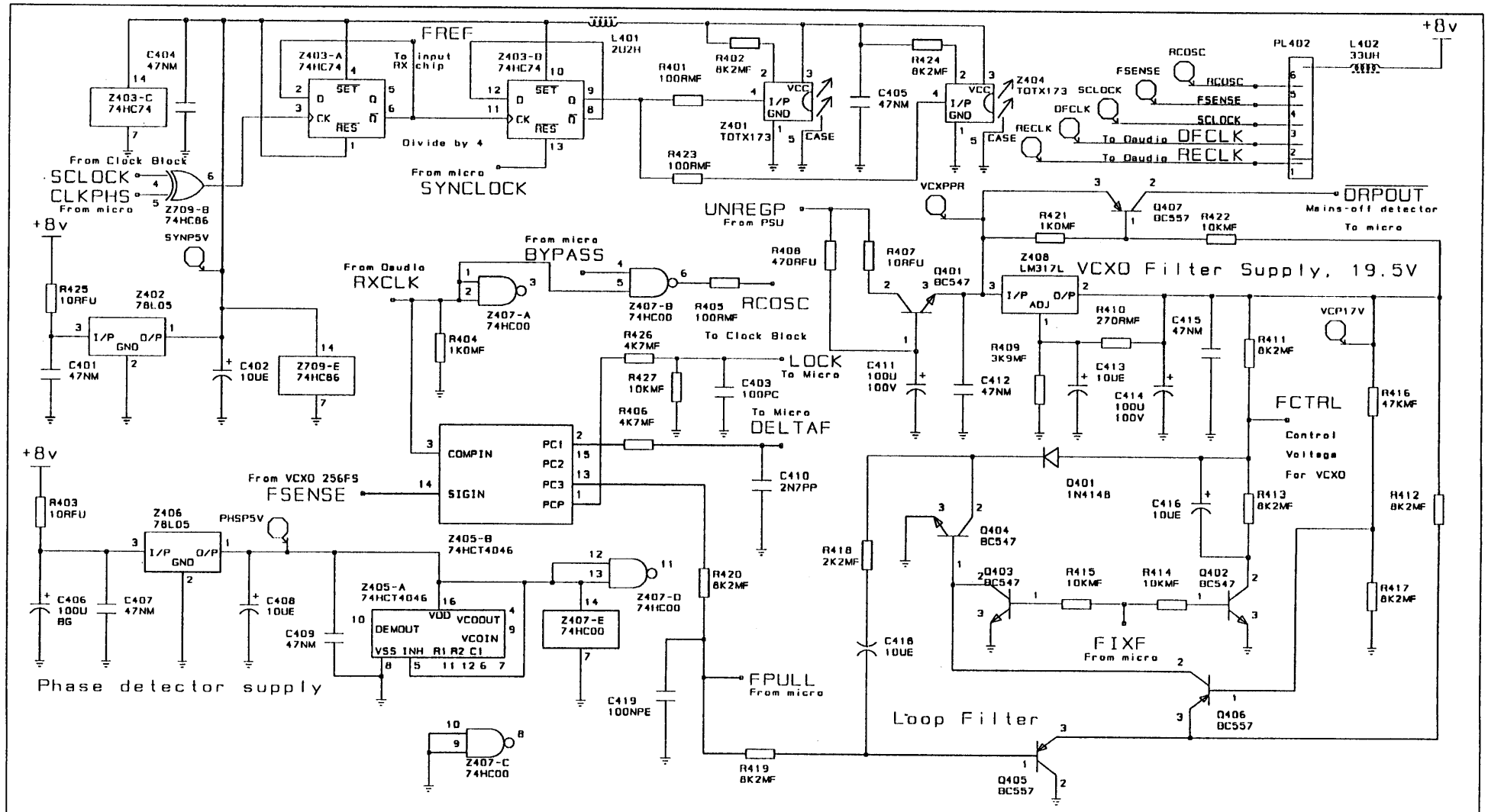
DRAWN BY SJB DATE 14-9-93

DRAWN WITH REFERENCE TO BS 308

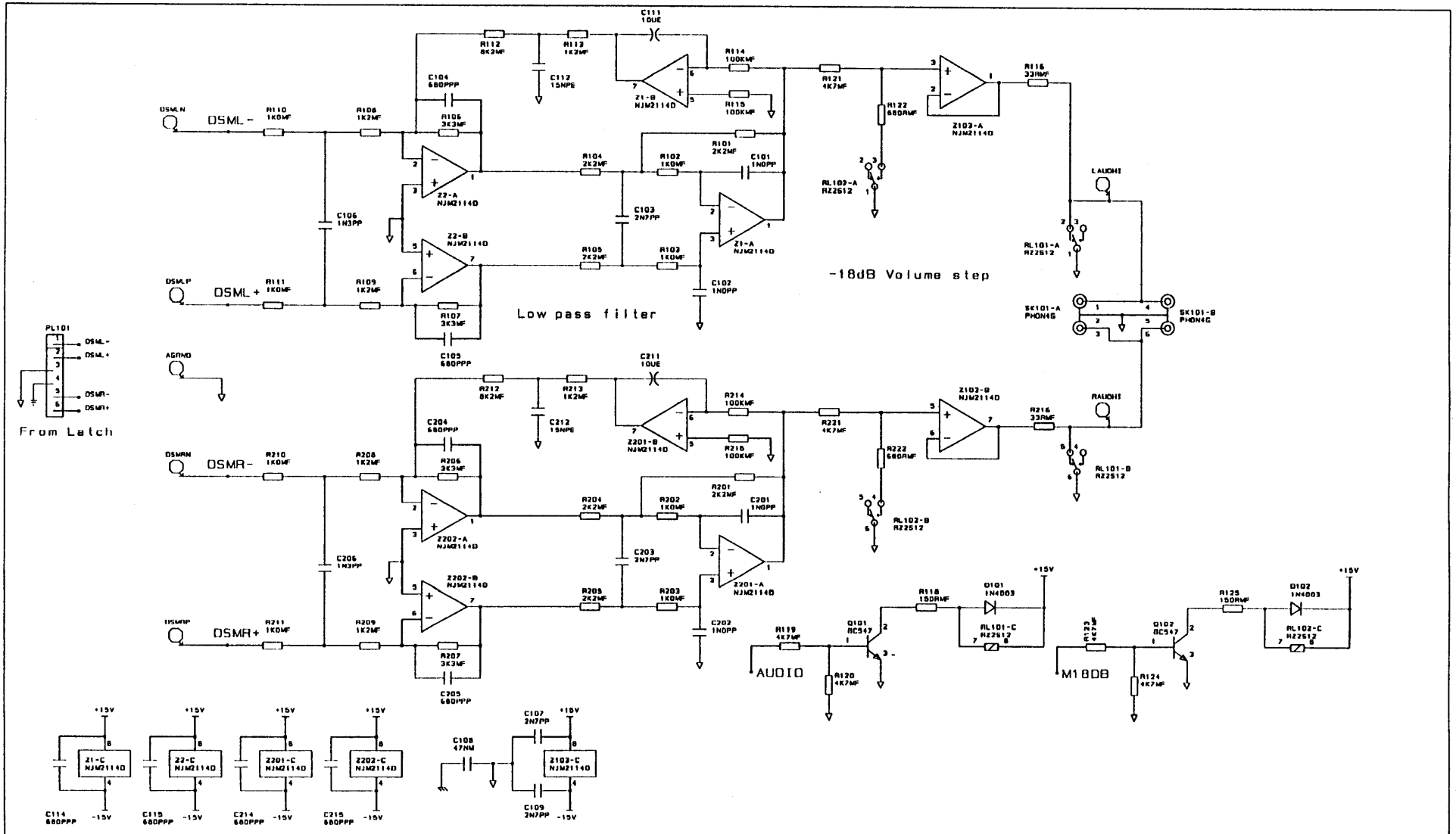
CHECKED BY DATE

SHT 2 OF 2

PART/ORG No. L702CT2



ARCAM A & R CAMBRIDGE LTD. WATERBEACH CAMBRIDGE CB5 9PB	DRAWING TITLE Clock Control Unit and PLL#2 L701CT3.CSD			
		2	SJB	27-7-94	R409 was 3K3, now 3K9 R413 was 12K, now 8K2	94/061
		1	SJB	21-6-94		
		ISSUE	INITIALS	DATE	DESCRIPTION OF CHANGE	ECO No
		DRAWING TYPE Circuit Digram			DRAWN WITH REFERENCE TO BS 308	
ALL DIMENSIONS IN MILLIMETERS UNLESS OTHERWISE STATED	ORIGINAL SCALE A3	DRAWN BY SJB	DATE 16-09-93	CHECKED BY	DATE	
TOLERANCES		SHT 3 OF 7		PART/ORG No. L701CT3		



ARCAM A & R CAMBRIDGE WATERBEACH CAMBRIDGE CB5 9PB	DRAWING TITLE ANALOGUE FILTER L701CT2.CSD	1	SJB	21-6-94
		ISSUE	INITIALS	DATE
		DESCRIPTION		ECO No.
		DRAWING TYPE Circuit Diagram		
ALL DIMENSIONS IN MILLIMETERS UNLESS OTHERWISE STATED	ORIGINAL A3 SCALE	DRAWN BY SJB	DATE 16-09-93	CHECKED BY / DATE
TOLERANCES		SHT 2	OF 7	PART/DRG No L701CT2